Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Previously presented) An integrated circuit, comprising:

an array of ferroelectric memory cells, each cell having a capacitor stack having a single ferroelectric core layer with a crystallization in the (001) family, wherein at least 40% of the domains of the single ferroelectric core layer are functionally oriented with respect to the capacitor stack, and wherein at least one of the capacitor stacks comprises a conductive contact formed thereover or thereunder, or both, and wherein the conductive contact has a cross section near a contact portion with the top portion of the stack, the bottom portion of the stack, or both, that is about as large or larger than that of the ferroelectric cores.

2. (Original) The integrated circuit of claim 1, wherein from about 45 to about 75% of the domains are functionally oriented with respect to the capacitor stack.

3. (Original) The integrated circuit of claim 1, wherein the ferroelectric cores are PZT cores and the PZT of each core has a switched polarization of at least about 60 $\mu C/cm^2$.

4. (Previously presented) The integrated circuit of claim 1, further comprising:

a dielectric layer covering the array of memory cells, the dielectric layer having a conductive contact over each ferroelectric core, the conductive contacts each having a cross section about as large or larger than that of the ferroelectric cores.

5. (Original) The integrated circuit of claim 1, wherein electrodes adjacent opposing sides of the ferroelectric cores have a collective thickness of at least about 200 nm thick.

6. (Previously presented) The integrated circuit of claim 1, wherein each of the capacitor stacks are formed over conductive contacts, the conductive contacts each having a cross section near their top that is about as large or larger than that of the ferroelectric cores.

7-20. (cancelled)

21. (New) The integrated circuit of claim 1, further comprising:

a dielectric layer covering the array of memory cells, the dielectric layer having a conductive contact over each ferroelectric core, the conductive contacts each having a cross section about as large or larger than that of the ferroelectric cores and extending through said dielectric layer to a metal interconnect layer.